RF LDMOS Power Transistor Technology For Pulsed L-Band Transmitters

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Over the last 10 years, the RF LDMOS (lateral double-diffused metal-oxide-semiconductor) power transistor has become the technology of choice for applications in the wireless base station infrastructure market. Due to its excellent linearity, high gain and efficiency, and power density exceeding 0.5W/mm, RF LDMOS is also a technology suitable for primary and secondary pulsed radar applications. This paper reports on the development of an RF LDMOS specifically designed and optimized for pulsed applications.

From Si-BJT To LDMOS

Avionics and conventional radar transmitters, where the output power of multiple transistors is combined, impose strict requirements on the characteristics of transistors. These requirements are as follows:

- Adequate gain, so at least four (and preferably six or more) devices can be driven in parallel.
- A minimum of 3:1 load mismatch tolerance to prevent burnout during tuning.
- The ability to remain stable under 2:1 mismatch.
- Phase stability, which is critical to the Doppler sensitivity of the system.

Phased array radars (PAR) have similar requirements, except gain can be lower since no circuit-level combining occurs in the transmitter. The silicon bipolar junction transistor (Si-BJT) is the workhorse of all modern radar designs operating below 3.5 GHz. Typically, a 100 W BJT with 9 dB gain, such as the Integra Technologies IB3135M100[1], drives six devices combined together to deliver over 600 W output power. In "High Power S-band Solid-State Amplifiers for Surveillance and Traffic Control Radars"[2], a 150 W, 7.5 dB gain, Si-BJT drives four of the same for 550 W combined output power, in the 2.7 to 2.9 GHz band, for the design of a 1.8 kW high-power amplifier (HPA). The authors chose IB2729M150 as their preferred Si-BJT transistor.

Technology computer aided device (TCAD) simulation tools have shortened development and optimization cycles and increased power density to 0.5 W/mm of emitter periphery at 3.5 GHz. However, spurred by the huge expansion of the wireless infrastructure market and its high-linearity requirements, the silicon-based RF LDMOS power transistor technology has emerged and evolved over the last 10 years with impressive performance in the 2.1 GHz range[3, 4, 5]. Mainly driven by the base stations market, typical RF figures of merit for LDMOS transistors report a power density of 0.82 W/mm, 14.5 dB gain, and peak efficiency in the mid 50% range[4], or 0.9 W/mm, gain of 16.5 dB, and 62% peak efficiency[5], with improvements at each new generation. Nowadays, RF LDMOS is a very mature and robust technology with performance in many respects superior to the BJT, and its penetration into the avionics, military, and defense applications markets is currently a very realistic proposition.

Unlike the BJT, which has been around since the 1970s, LDMOS is a relatively recent technology, developed between the late 1980s and early 1990s, which has become the technology of choice for base station applications. Due to its higher gain and efficiency, and most importantly superior linearity, LDMOS has completely replaced the BJT as the technology of choice for linearity critical applications such as the wireless infrastructure base station business[6]. Most of the development, optimization, and design evolution of the LDMOS transistor has been driven by the linearity requirements of infrastructure applications[7]. However, LDMOS is also a viable candidate for avionics, as well as L- and S-band radar applications. Optimized for class B pulsed operation, LDMOS is beginning to challenge the supremacy of the BJT in the avionics and radar market segments.

Integra Technologies has developed its fifth-generation RF LDMOS, designed and optimized entirely for pulsed avionics and L-band radar applications.

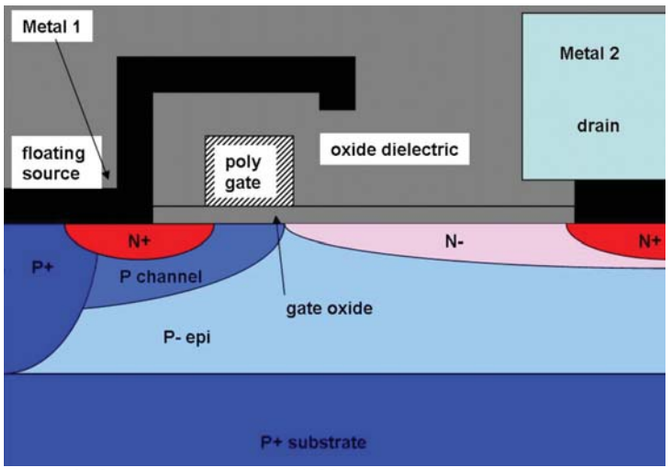

FIGURE 1: CROSS SECTION OF AN LDMOS DESIGN WITH FARADAY SHIELD. (DRAWING IS NOT TO SCALE.)

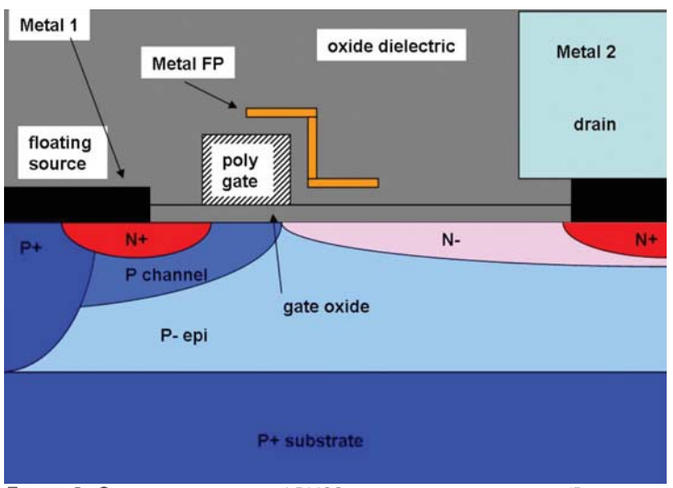

FIGURE 2: CROSS SECTION OF AN LDMOS DESIGN WITH FIELD PLATE. (DRAWING IS NOT TO SCALE.)

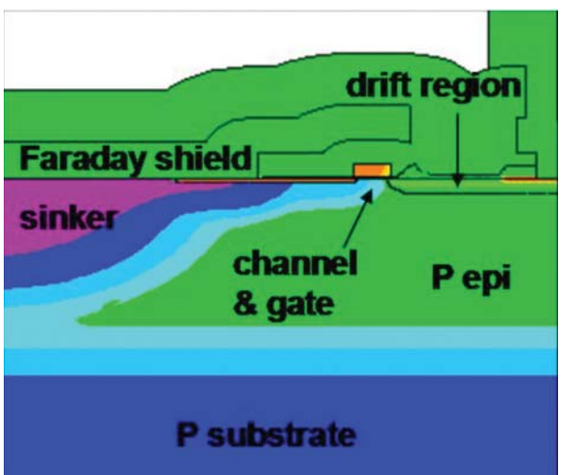

FIGURE 3: TCAD CROSS-SECTION OF INTEGRA TECHNOLOGIES' LDMOS DESIGN WITH FARADAY SHIELD. GEOMETRY FEATURES AND DOPING LEVELS ARE OMITTED FOR CONFIDENTIALITY PURPOSES.

LDMOS Designs

There are two main categories of LDMOS designs. One relies on a grounded Faraday shield to isolate the gate from the drain and therefore reduce the feedback capacitance Cdg, mainly used with gate lengths longer than 0.5 um, as shown in *Figure 1*. Another design, typical of transistors with sub-0.5 um gate length, makes use of a grounded field plate to reduce both feedback capacitance Cdg and Idq drift. *Figure 2* shows a typical cross section of this design. Because the field plate is closer to the drain edge of the channel, it is most effective in reducing feedback capacitance and Idq drift at the same time5. However, this design leads to an increase in gate-to-source capacitance Cgs, since the metal plate is closer to the gate. Integra Technologies, with its gold metallization, has adopted the design shown in *Figure 1*. A TCAD-generated cross section, also used for the process flow design and the transistor optimization, is shown in *Figure 3*. Please note that geometry features and doping level information have been omitted for confidentiality purposes.

Since the source to drain pitch size of a one-finger LDMOS cell is larger than the base to emitter pitch size in the BJT, the junction temperature is maintained below 200 C, even with LDMOS power densities higher than 0.5 W/mm. Its advantages include the source at the back of the wafer, therefore easily mounted on a grounded package that does not require expensive packages with BeO (beryllium oxide) insulation. The back-wafer source also provides low source inductance, which also helps to achieve LDMOS's superior gain performance compared to BJT.

Low RDSon (drain to source on resistance) is achieved through advanced drain engineering of the drift region, which also results in excellent efficiency for pulsed class B power amplifiers[7]. Major OEMs (original equipment manufacturers) focused on infrastructure base stations and WiMAX applications run LDMOS production lines in state-of-the-art CMOS fabs with two to four Al (aluminum) or AlCu (aluminum copper) based metal layers. Integra Technologies, with its focus on military and defense markets, manufactures LDMOS transistors optimized for pulsed applications in their on-site fab using two or more all-gold metal layers. These features are already incorporated in their lineup of high-performance BJT and VDMOS (vertical diffused metal-oxide-semiconductor) products.

Results And Discussions

Integra Technologies has developed and characterized LDMOS transistors for avionics applications at 1030/1090 MHz as used in various avion-

ics systems. RF data for two LDMOS samples from the same wafer, with 16 mm and 60 mm gate periphery, are reported and discussed. Both have 85 V breakdown and are suitable for operation at 26, 32, or 36 V. Using a 32 us pulsed signal with 2% duty cycle, the 16 mm die has a saturated power of about 15 W, with 15 dB peak gain and above 50% drain efficiency, as shown in *Figure 4*. The quiescent current is 5 mA. This data shows a power density around 1 W/mm, even with 26 V operation. Operation with a power supply at 32 or 36 V will further increase the power density[7].

Under similar conditions, the 60 mm die has a saturated power of about 35 W, with 13 dB peak gain and above 50% drain efficiency, as shown in *Figure 5*. The quiescent current in this case is 10 mA. The data shows a power density around 0.6 W/mm at 26 V operation. Higher supply voltage will give higher output power. Multiple dies can also be packaged together for chips with higher output power ratings. These RF figures of merit are very competitive with respect to the BJT, such as the IB1011 family of avionics BJT transistors[1].

Through further drain engineering, it is possible to boost the above reported RF performance. For instance, another 16 mm die from a different wafer with different process conditions was tested, also at 26 V operation and 5 mA quiescent current, and has 17 W saturated output power, or >1.1 W/mm power density, with 16 dB peak gain and 60% drain efficiency, as reported in *Figure 6*. Breakdown voltage for this die is 80 V, still allowing for higher supply voltage operation.

In *Figures 7* and 8, we show pictures of the 16 mm and 60 mm dies in their respective packages. The right side of *Figure 7* shows a magnification of the die. Notice the tree-structured input and output feeding of grouped transistor fingers. This approach minimizes phase delays and internal mismatches between the several fingers that make up the larger die. The topology can be optimized to the particular size, power level, and intended frequency of operation of the transistor. To avoid electromigration-related failure, the width of the metal increases in the tree-structure going from the intrinsic transistor finger to the metal bonding pad.

Although LDMOS immunity to phase noise is not as good as in the BJT, it is expected that with the further optimization of the transistor design, specifically intended for pulsed operation, it is likely

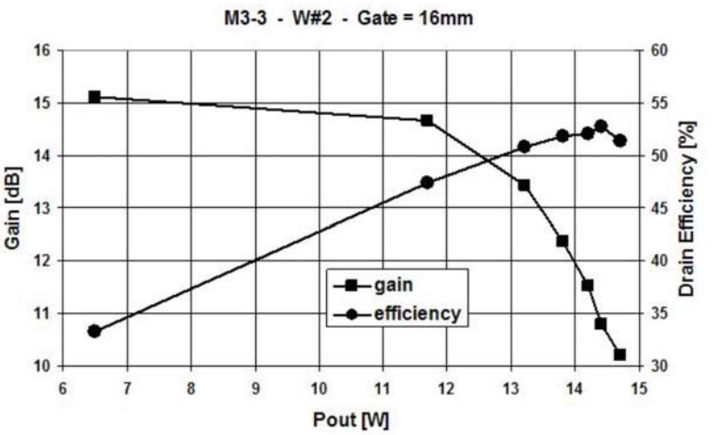

Figure 4: Pulsed data at 1030 MHz of gain and efficiency vs. output power for a 16 mm LDMOS die.

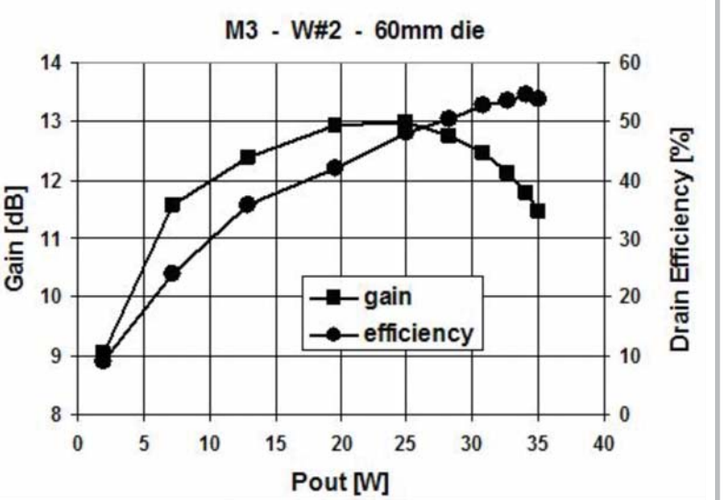

Figure 5: Pulsed data at 1030 MHz of gain and efficiency vs. output power for a 60 mm LDMOS die.

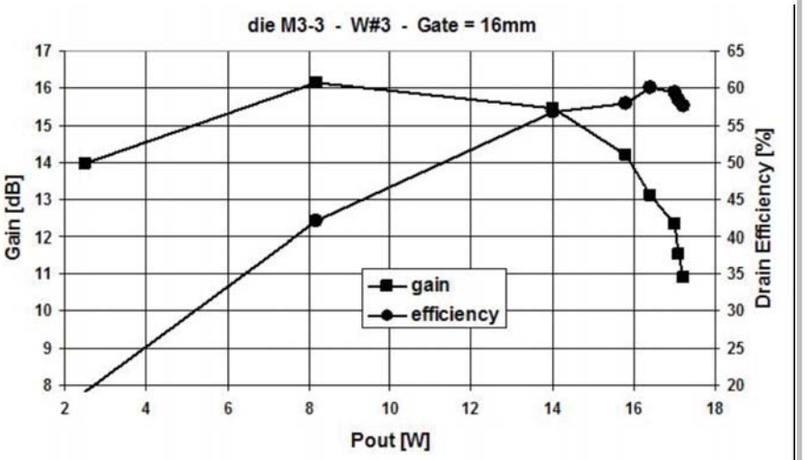

Figure 6: Pulsed data at 1030 MHz of gain and efficiency vs. output power for a 16 mm LDMOS die with a different process flow from what was shown in Figure 4.

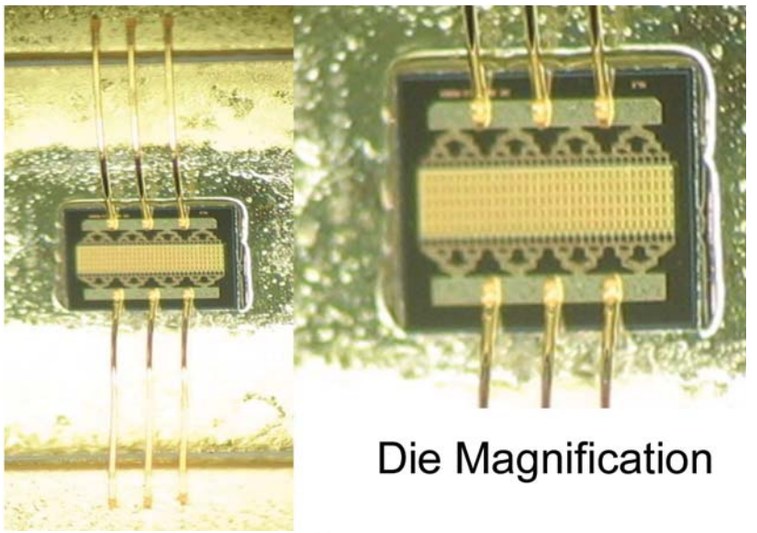

FIGURE 7: PICTURE OF A 16 MM LDMOS DIE.

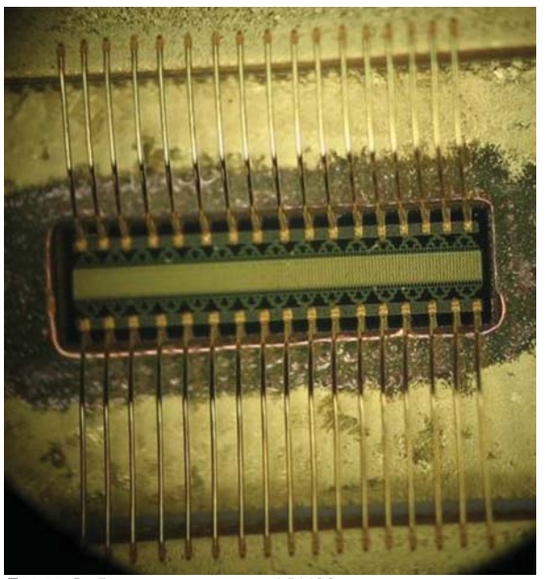

FIGURE 8: PICTURE OF A 60 MM LDMOS DIE.

that LDMOS will pose a serious threat to the BJT predominance in this market in the near future. Its ability to utilize less-expensive packages (no BeO insulation) and easier input drive circuits (being a voltage-controlled device) may further accelerate the LDMOS acceptance into the avionics and radar marketplace.

Conclusions

Integra Technologies has successfully developed and evaluated an all-gold LDMOS technology specifically designed to address requirements for avionics and radar applications. Unlike other LDMOS manufacturers that focus on the base stations infrastructure market, which require die design and optimization for maximum linearity, Integra's gold metallization ensures maximum reliability. And the company's focus on strictly military and defense markets allows the design and optimization of its LDMOS technology for maximum performance in pulsed applications.

Acknowledgments

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